In the claims:

Please amend claims 1, 3 and 22 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A semiconductor device comprising a plurality of layers, the semiconductor device comprising:

- a substrate having a first major surface,

- an inductive element fabricated on the first major surface of the substrate the inductive element comprising at least one conductive line,

- a plurality of tilling structures in at least one layer, the plurality of tilling structures arranged to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.

2. (Previously presented) A semiconductor device according to claim 1, the tilling structures being made from tilling structure material, wherein the plurality of tilling structures are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element is smaller than the amount of tilling structure material in an area farther away from the inductive element.

3. (Currently amended) A semiconductor device according to claim 1, wherein the tilling structures are located at different layers, tilling structures at each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element, and wherein the arrangement of the tilling structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics.

4. (Previously presented) A semiconductor device according to claim 3, wherein the geometrical pattern of tilling structures at two different layers is different in shape and/or orientation.

5. (Previously presented) A semiconductor device according to claim 3, wherein the tilling structures at different layers are electrically connected to each other.

6. (Previously presented) A semiconductor device according to claim 1, wherein the tilling structures are connected to a DC potential.

7. (Previously presented) A semiconductor device according to claim 1, wherein the tilling structures are a plurality of slender elongate elements.

8. (Previously presented) A semiconductor device according to claim 1, wherein the tilling structures are a plurality of substantially triangular elements.

9. (Previously presented) A semiconductor device according to claim 7, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.

10. (Previously presented) A semiconductor device according to claim 8, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.

11. (Previously presented) A semiconductor device according to claim 1, furthermore comprising a ground shield for shielding the inductive element from a further layer.

12. (Previously presented) A semiconductor device according to claim 11, wherein the further layer is the substrate.

13. (Previously presented) A semiconductor device according to claim 11, furthermore comprising connection means electrically connecting the plurality of tilling structures with the ground shield without creating a conductive loop.

14. (Previously presented) A semiconductor device according to claim 1, wherein the tilling structures are formed in a region other than a region directly below the inductive element.

15. (Previously presented) A semiconductor device according to claim 1, furthermore provided with a further passive element.

16. (Previously presented) A semiconductor device according to claim 15, wherein the further passive element is a capacitive element.

17. (Previously presented) A semiconductor device according to claim 16, wherein the capacitive element comprises two capacitor electrodes at least one of the capacitor electrodes being formed by a plurality of tilling structures.

18. (Previously presented) A semiconductor device according to claim 17, wherein a capacitor electrode formed by a plurality of tilling structures leads to a metal or polysilicon or active region density in the inductor vicinity respecting the design rules of advanced IC technologies.

19. (Previously presented) A semiconductor device according to claim 17, wherein one capacitor electrode of the capacitive element is formed by a ground shield.

20. (Previously presented) A semiconductor device according to claim 15, wherein the integration of the capacitive element with the inductive element is optimized to respect the metal pattern density in advanced silicon technologies.

21. (Previously presented) A semiconductor device according to claim 15, wherein the distance between the capacitive element and the inductive element is large enough to avoid a dominant fringe coupling between them.

22. (Currently amended) A method for providing an inductive element in a semiconductor device comprising a plurality of layers, the method comprising:

- providing a substrate having a first major surface,

- forming an inductive element above the first major surface of the substrate, the inductive element comprising at least one conductive line,

- providing a plurality of tilling structures in at least one layer to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.